**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**



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|---|---|---|
| In re the Application of | | TI-28917 |
| | Venkatesh Natarajan, et al. | Art Unit: 2823 |
| Serial No.: | 09/451,979 | Examiner: Julio J. Maldonado |
| Filed: | October 20, 1999 | Conf. No: 4880 |
| For: | A Method And Apparatus For Combining Memory Blocks For In Circuit Emulation | |

## LETTER TO THE OFFICIAL DRAFTSPERSON

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(a)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Ass't Commissioner for Patents, Washington, D.C. 20231 on
April 8, 2003

Robin E. Barnum

Ass't Commissioner for Patents
Washington, D.C. 20231

Sir:

Please find enclosed the formal drawings for the subject case. Charge any necessary fees to Texas Instruments Incorporated, Deposit Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,

Gerald E. Laws
Attorney for Applicant
Reg. No. 39,268

Texas Instruments Incorporated
P.O. Box 655474, MS 3999